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(Original Signature of Member)

119TH CONGRESS  
1ST SESSION

**H. R.** \_\_\_\_\_

To amend the Internal Revenue Code of 1986 to add qualified semiconductor design expenditures to the advanced manufacturing investment credit.

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IN THE HOUSE OF REPRESENTATIVES

Mr. MOORE of Utah introduced the following bill; which was referred to the Committee on \_\_\_\_\_

\_\_\_\_\_  
**A BILL**

To amend the Internal Revenue Code of 1986 to add qualified semiconductor design expenditures to the advanced manufacturing investment credit.

1 *Be it enacted by the Senate and House of Representa-*  
2 *tives of the United States of America in Congress assembled,*

3 **SECTION 1. SHORT TITLE.**

4 This Act may be cited as the “Semiconductor Tech-  
5 nology Advancement and Research Act of 2025” or the  
6 “STAR Act of 2025”.

1 **SEC. 2. QUALIFIED SEMICONDUCTOR DESIGN EXPENDI-**  
2 **TURES ADDED TO ADVANCED MANUFAC-**  
3 **TURING INVESTMENT CREDIT.**

4 (a) IN GENERAL.—Section 48D of the Internal Rev-  
5 enue Code of 1986 is amended—

6 (1) in subsection (a), by striking “an amount  
7 equal to” and all that follows through the period and  
8 inserting “, with respect to an eligible taxpayer, an  
9 amount equal to the sum of—

10 “(1) 25 percent of the qualified investment for  
11 such taxable year with respect to any advanced man-  
12 ufacturing facility of such taxpayer, and

13 “(2) 25 percent of the qualified semiconductor  
14 design expenditures paid or incurred by such tax-  
15 payer during the taxable year.”,

16 (2) by redesignating subsections (c), (d), and  
17 (e) as subsections (e), (f), and (g), respectively,

18 (3) by inserting after subsection (b) the fol-  
19 lowing new subsections:

20 “(c) QUALIFIED SEMICONDUCTOR DESIGN EXPENDI-  
21 TURES.—

22 “(1) IN GENERAL.—For purposes of subsection  
23 (a)(2), the term ‘qualified semiconductor design ex-  
24 penditures’ means the sum of the following amounts  
25 which are paid or incurred by the taxpayer during

1 the taxable year in carrying on any trade or business  
2 of the taxpayer for—

3 “(A) in-house semiconductor design ex-  
4 penses for semiconductor design conducted in  
5 the United States, and

6 “(B) contract design expenses for semicon-  
7 ductor design conducted in the United States.

8 “(2) IN-HOUSE SEMICONDUCTOR DESIGN EX-  
9 PENSES.—

10 “(A) IN GENERAL.—The term ‘in-house  
11 semiconductor design expenses’ means—

12 “(i) any wages paid or incurred to an  
13 employee for qualified services performed  
14 by such employee,

15 “(ii) any amount paid or incurred for  
16 supplies used in the conduct of qualified  
17 semiconductor design, and

18 “(iii) under regulations prescribed by  
19 the Secretary, any amount paid or in-  
20 curred to another person for the right to  
21 use computers in the conduct of qualified  
22 semiconductor design.

23 Clause (iii) shall not apply to any amount to  
24 the extent that the taxpayer (or any person  
25 with whom the taxpayer must aggregate ex-

1           penditures under paragraph (7) receives or ac-  
2           crues any amount from any other person for  
3           the right to use substantially identical personal  
4           property.

5           “(B) QUALIFIED SERVICES.—The term  
6           ‘qualified services’ means services consisting  
7           of—

8                   “(i) engaging in qualified semicon-  
9                   ductor design, or

10                   “(ii) engaging in the direct super-  
11                   vision or direct support of design activities  
12                   which constitute qualified semiconductor  
13                   design.

14           If substantially all of the services performed by  
15           an individual for the taxpayer during the tax-  
16           able year consists of services meeting the re-  
17           quirements of clause (i) or (ii), the term “quali-  
18           fied services” means all of the services per-  
19           formed by such individual for the taxpayer dur-  
20           ing the taxable year.

21           “(C) SUPPLIES.—The term ‘supplies’ has  
22           the meaning given such term in section  
23           41(b)(2)(C).

1           “(D) WAGES.—The term ‘wages’ has the  
2           meaning given such term in section  
3           41(b)(2)(D).

4           “(3) CONTRACT DESIGN EXPENSES.—

5           “(A) IN GENERAL.—The term “contract  
6           design expenses” means 100 percent of any  
7           amount paid or incurred by the taxpayer to any  
8           person (other than an employee of the tax-  
9           payer) for qualified semiconductor design.

10           “(B) PREPAID AMOUNTS.—If any contract  
11           design expenses paid or incurred during any  
12           taxable year are attributable to qualified semi-  
13           conductor research to be conducted after the  
14           close of such taxable year, such amount shall be  
15           treated as paid or incurred during the period  
16           during which the qualified semiconductor design  
17           is conducted.

18           “(4) TRADE OR BUSINESS REQUIREMENT DIS-  
19           REGARDED FOR IN-HOUSE DESIGN EXPENSES OF  
20           CERTAIN STARTUP VENTURES.—In the case of in-  
21           house semiconductor design expenses, a taxpayer  
22           shall be treated as meeting the trade or business re-  
23           quirement of paragraph (1) if, at the time such in-  
24           house semiconductor design expenses are paid or in-  
25           curred, the principal purpose of the taxpayer in

1 making such expenditures is to use the results of the  
2 design in the active conduct of a future trade or  
3 business—

4 “(A) of the taxpayer, or

5 “(B) of 1 or more persons who with the  
6 taxpayer are treated as single taxpayer under  
7 paragraph (7).

8 “(5) QUALIFIED SEMICONDUCTOR DESIGN.—

9 “(A) IN GENERAL.—The term ‘qualified  
10 semiconductor design’—

11 “(i) means the development (or direc-  
12 tion of the development) of product design,  
13 design specifications, trade secrets, tech-  
14 nology, or other intellectual property for  
15 the purpose of semiconductor manufac-  
16 turing, substantially all of the activities of  
17 which constitute elements of a process of  
18 experimentation for a purpose described in  
19 subparagraph (B)(i), and

20 “(ii) does not include any activity de-  
21 scribed in subparagraph (B)(ii).

22 “(B) PURPOSES FOR WHICH RESEARCH  
23 MAY QUALIFY FOR CREDIT.—For purposes of  
24 subparagraph (A)—

1                   “(i) IN GENERAL.—Semiconductor de-  
2                   sign shall be treated as conducted for a  
3                   purpose described in this paragraph if it  
4                   relates to—

5                               “(I) a new or improved function,

6                               “(II) performance, or

7                               “(III) reliability or quality.

8                   “(ii) CERTAIN PURPOSES NOT QUALI-  
9                   FIED.—Semiconductor design shall in no  
10                  event be treated as conducted for a pur-  
11                  pose described in this paragraph if it is  
12                  conducted for purposes of—

13                              “(I) style, taste, cosmetic, or  
14                              other design factors unrelated to a  
15                              purpose described in clause (i),

16                              “(II) design after the commence-  
17                              ment of commercial production of the  
18                              semiconductor, unless such design is  
19                              related to firmware, software, or man-  
20                              ufacturing process activities that  
21                              would otherwise meet the require-  
22                              ments of clause (i),

23                              “(III) duplication of an existing  
24                              semiconductor product (in whole or in  
25                              part) from a physical examination of

1 the semiconductor itself or from  
2 plans, blueprints, detailed specifica-  
3 tions, or publicly available information  
4 with respect to such semiconductor, or  
5 “(IV) surveys or studies related  
6 to—

7 “(aa) efficiency,

8 “(bb) management function  
9 or techniques,

10 “(cc) market research, test-  
11 ing, or development, including  
12 advertising and promotions,

13 “(dd) routine data collec-  
14 tion, or

15 “(ee) routine or ordinary  
16 testing or inspection for quality  
17 control.

18 “(6) UNITED STATES.—For purposes of this  
19 subsection, the term ‘United States’ includes the  
20 possessions of the United States.

21 “(7) AGGREGATION OF EXPENDITURES.—For  
22 purposes of this subsection, in determining the  
23 amount of qualified semiconductor design expendi-  
24 tures, rules similar to the rules of section 41(f)(1)  
25 shall apply.



1           “(d) COORDINATION WITH CREDIT FOR INCREASING  
2 RESEARCH EXPENDITURES.—Any qualified semicon-  
3 ductor design expenditures for which a credit is allowed  
4 under this section shall not be taken into account for pur-  
5 poses of determining the credit allowable under section 41  
6 for such taxable year.”, and

7           (4) by amending subsection (g) (as so redesignig-  
8 nated) to read as follows; by inserting “or qualified  
9 semiconductor design expenditures paid or incurred  
10 after December 31, 2026” before the period.

11          “(g) TERMINATION OF CREDIT.—The credit allowed  
12 under this section shall not apply to—

13           “(1) property the construction of which begins  
14 after December 31, 2036, or

15           “(2) qualified semiconductor design expendi-  
16 tures paid or incurred after December 31, 2036.”.

17          (b) CONFORMING AMENDMENT.—Section 56A(e)(9)  
18 of the Internal Revenue Code of 1986 is amended by strik-  
19 ing “48D(d)” and inserting “48D(f)”.

20          (c) EFFECTIVE DATE.—The amendments made by  
21 this section shall apply to amounts paid or incurred after  
22 the date of the enactment of this Act.